REMARKS

The following remarks are made in response to the Office Action mailed September 22, 2004. Claims 1-5 and 17-33 were rejected. Claims 6-16 have been objected to. With this Response, claims 1, 6, 17-18, 21-22, and 31 have been amended and claim 34 has been added. Claims 1-34 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 112

The Examiner rejected claims 17-30 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Accordingly, Applicant has amended independent claim 17 to remove use of the vague and indefinite verb "can" and believes independent claim 17 to be in compliance with the requirements of 35 U.S.C. § 112, second paragraph. As such, Applicant respectfully requests that the rejection of claims 17-30 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 1-5, 17-21, and 31-33 under 35 U.S.C. § 102(b) as being anticipated by Hampel et al. U.S. Patent No. 6,310,814 ("Hempel"). Independent claim 1 has been amended to clarify that the timing signals provided via the bus are global timing signals and that each tracking circuit, in response to receiving an array address for its associated array, couples its associated array to the bus so that only its associated array receives and responds to a sequence of global timing signals constituting a transaction with the bank. As such, the tracking circuits of the present invention do not generate timing signals, but function as gates to pass sequences of global timing signals constituting a bank transactions to their associated array based on an array address associated with each of the sequences of global timing signals.

Hampel does not disclose tracking circuits that couple an associated array to a bus for receiving a sequence of global timing signal, but instead teaches reducing overhead associated with refresh operations by pipelining refresh operations through sequencing of active refresh and

precharge refresh commands, wherein the sequence of timings signals is generated at each bank by the corresponding row address circuit (column 6, lines 23-24). This is evidenced by the timing diagram of Figure 3 and at column 6, lines 13-22, wherein the reduction in refresh overhead is described as being "achieved by combining a command interface 21 that supports receipt of pipelined refresh command sequences with an RDRAM core *that includes logic for performing row operations (i.e., precharge and active operations) on respective storage banks independently of one another.*

As such, Hampel does not teach or suggest a tracking circuit that couples an associated array to a bus for receiving a sequence of global timing signals based on an array address. Similar limitations are included in claims 17 and 31. Accordingly, Applicant believes the above rejections of claims 1, 17, and 31 under 35 U.S.C. § 102(b) as being anticipated by Hampel should be withdrawn.

Dependent claims 2-5, 18-21, and 32-33 depend directly or indirectly from independent claims 1, 17, and 31, respectively. Accordingly, dependent claims 2-5, 18-21, and 32-33 are also believed allowable over Hampel.

Dependent claims 18 and 21 have been amended to provide proper antecedent basis under 35 U.S.C. § 112.

Allowable Subject Matter

The Examiner objected to claims 6-16 for being dependent upon a rejected base claim, but as being allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

The Examiner objected to claims 22-30 for being dependent upon a rejected base claim, but as being allowable if rewritten in independent form including all limitations of the base claim and any intervening claims and if rewritten to overcome the rejections under 35 U.S.C. §112.

Applicant agrees with the Examiner's conclusions regarding patentability without necessarily agreeing with or acquiescing in the Examiner's reasoning. In particular, Applicant believes that the claims are allowable because prior art fails to teach, anticipate or render obvious the invention as claimed, independently of how the invention is paraphrased.

Accordingly, Applicant has rewritten claims 6 and 22 in independent form and to overcome the rejection under 35 U.S.C. §112. Allowance of these claims and the claims dependent therefrom is respectfully requested.

Added Claim

Added independent claim 34 recites a method of increasing bandwidth of a semiconductor memory having a plurality of arrays and includes the allowable subject matter of claims 6 and 22. Applicant believes claim 34 to be allowable over the art of record.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-34 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-34 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 22nd day of December, 2004.

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